OKI semiconductor

MSM51C262

High Performance Low Power 64K x 4 Multi-port Memory with Fast Page Mode

GENERAL DESCRIPTION

The OKI MSM51C262 is a high speed 65,536 x 4-bit multiport CMOS dynamic memory. The two ports, random access and serial access, are configured to offer optimum flexibility in graphics and other systems that require an interface between a processor and a high speed serial data channel such as a CRT or graphics display device.

The organization of the random access port of the MSM51C262 is exactly like, a 64K x 4 CMOS DRAM. Additional functions such as transfer between RAM and SAM (serial access memory) use otherwise unused states of the $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ signals sampled at the falling edge of RAS at the beginning of a cycle.

SAM is organized as 256 x 4 bits that can be read or written at high speed. The contents of SAM can be loaded into RAM, and the contents of a selected RAM row (256 x 4) can be loaded into SAM. Except when transferring data between one another, SAM and RAM operate in an asynchronous manner. The transfer from RAM to SAM or SAM to RAM also refreshes the transferred row in the RAM.

In a RAM to SAM load cycle, 8 bits are needed to specify which of the 256 rows is to be transferred. The state of the address lines at the falling edge of $\overline{CAS}$ is used to specify the starting point in SAM where data is to be written or read. The static mechanization of the SAM (allowed by CMOS) does not require refreshing. The first access to SAM, either read or write, is to the location specified at $\overline{CAS}$ time in the previous cycle, and subsequent accesses continue in an increasing address direction, module 256.

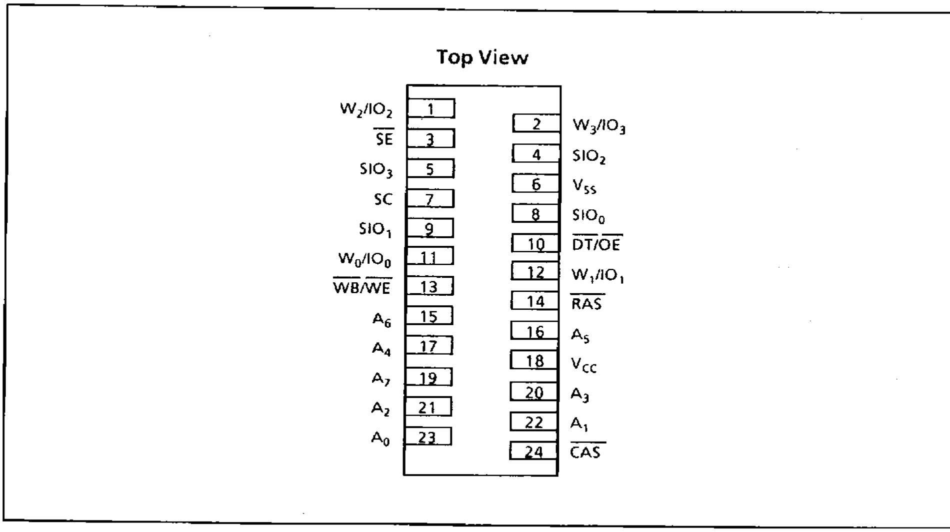
The MSM51C262 is processed using OKI's CMOS silicon gate process technology. This advanced CMOS processing allows memory devices to be fabricated with lower operating current and higher performance than comparable NMOS designs. All I/O signals are TTL compatible. Input and I/O capacitances are significantly lowered to enhance system performance.

FEATURES

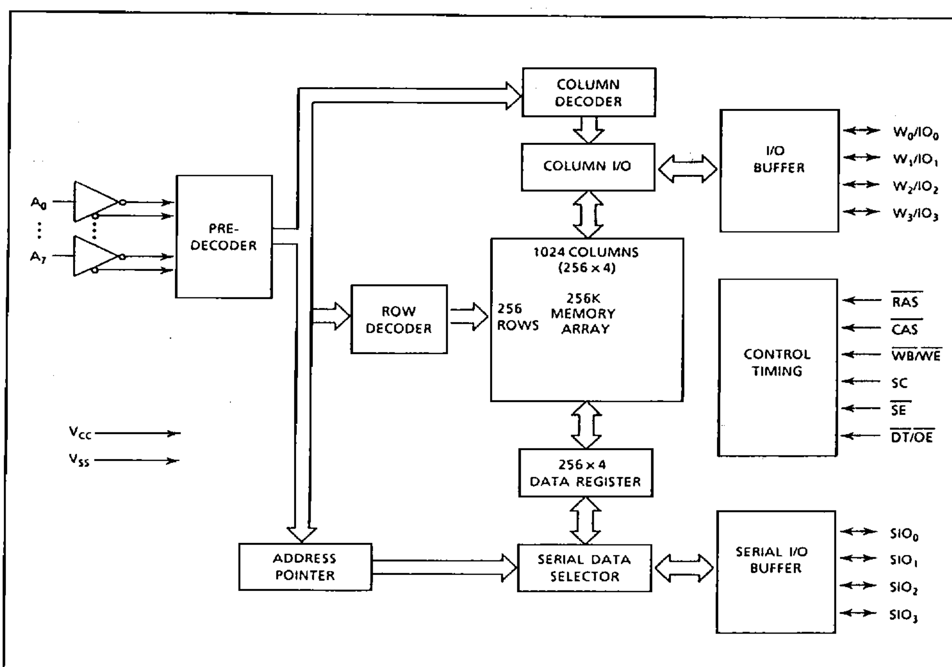
- Low power dissipation for MSM51C262-12
  - RAM port operating alone – 50 mA
  - SAM port operating alone – 35 mA
  - RAM/SAM operating 5 together – 85 mA
- Low CMOS standby current – 6 mA
- Fast Page Mode access, $\overline{RAS}$-Only Refresh, and $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Bi-directional data transfer between RAM and SAM with real-time operation.
- Bit-masked Write function on RAM port for additional flexibility.
- 256 Refresh cycle/4 ms.
- Standard package is 24 pin 400 mil Plastic ZIP.

High Performance MSM51C262	– 80	– 10	– 12
Max. $\overline{RAS}$ Access Time (t_{RAC})	80 ns	100 ns	120 ns
Max. Column Address Time (t_{CAA})	40 ns	45 ns	55 ns
Min. Fast Column Mode Cycle Time (t_{PC})	55 ns	60 ns	70 ns
Min. Read/Write Cycle Time (t_{RC})	145 ns	175 ns	205 ns
Min. Serial Port Cycle Time (t_{SCC})	30 ns	35 ns	40 ns

24 LEAD PLASTIC ZIP PIN CONFIGURATION



BLOCK DIAGRAM



11

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Ambient Temperature Under Bias	0 to 70	°C
Storage Temperature (Plastic)	– 55 to + 125	°C
Voltage on any Pin Except V_{CC} Relative to V_{SS}	– 1.0 to + 7.0	V
Voltage on V_{CC} Relative to V_{SS}	– 1.0 to + 7.0	V
Data Output Current	50	mA
Power Dissipation	1.0	W

* Operation at or above ABSOLUTE MAXIMUM RATINGS can adversely affect device reliability.

AC TEST CONDITIONS

Conditions	Value	Unit
Input Rise Levels	0 to 3.0	V
Input Rise and Fall Times	5 between 0.8 V and 2.4 V	ns
Input Timing Reference Levels	0.8 and 2.4	V
Output Timing Reference Levels	0.8 and 2.4	V
Output Load (RAM Port)	2 TTL (and 100)	pF
Output Load (SAM Port)	2 TTL (and 50)	pF

CAPACITANCE*

T_A = 25°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance		5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$, SC, $\overline{DT}/\overline{OE}$ Capacitance		8	pF
C_{OUT}	I/O Capacitance		7	pf

* Capacitance is sampled and not 100% tested.

DC CHARACTERISTICS (1)

(T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.)

Parameter	Symbol	Conditions	Access Time	MSM51C262 Min.	MSM51C262 Max.	Unit	Notes
Input Leakage Current (Any Input Pin)	I_{LI}	$V_{SS} < V_{IN} < V_{CC}$		−10	10	μA	
Output Leakage Current (For High-Z State)	I_{LO}	$V_{SS} < V_{OUT} < V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ and $\overline{SE}$ at V_{IH}		−10	10	μA	
V_{CC} Supply Current	I_{CC1}	$\overline{RAS}$/$\overline{CAS}$ Cycling, SAM Port TTL Standby t_{RC} (min.), SC = V_{IL}	80		70	mA	2, 3
			100		60		
			120		50		
V_{CC} Supply Current, TTL Stanbdy	I_{CC2}	RAM/SAM Ports TTL Standby RAS, CAS at V_{IH}, I/O > V_{SS} SC = V_{IL}			8	mA	
V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH} SAM Port TTL Standby t_{RC} (min.), SC = V_{IL}	80		70	mA	2, 3
			100		60		
			120		50		
V_{CC} Supply Current, Page Mode Operation	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM Port TTL Standby t_{PC} (min.), SC = V_{IL}	80		60	mA	2, 3
			100		50		
			120		40		
V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	I_{CC5}	$\overline{RAS}$/$\overline{CAS}$ Cycling, SAM Port TTL Standby t_{RC} (min.), SC = V_{IL}	80		70	mA	2, 3
			100		60		
			120		50		
V_{CC} Supply Current, RAM/SAM Transfer Mode	I_{CC6}	$\overline{RAS}$/$\overline{CAS}$ Cycling, SAM Port TTL Standby t_{RC} (min.), SC = V_{IL}	80		75	mA	2, 3
			100		65		
			120		55		
V_{CC} Supply Current, Both Ports Active	I_{CC7}	$\overline{RAS}$/$\overline{CAS}$ Cycling, SAM Port Active t_{RC} (min.), t_{SCC} (min.)	80		120	mA	2, 3
			100		100		
			120		85		
V_{CC} Supply Current, SAM-Only Operation	I_{CC8}	$\overline{RAS}$/$\overline{CAS}$ at V_{IH}, I/O > V_{SS} SAM Port Active t_{SCC} (min.)	80		50	mA	2
			100		40		
			120		35		
V_{CC} Supply Current, $\overline{RAS}$-Only Refresh and SAM Active	I_{CC9}	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH}, SAM Port Active t_{RC} (min.), t_{SCC} (min.)	80		120	mA	2, 3
			100		100		
			120		85		
V_{CC} Supply Current, Page Mode Operation and SAM Active	I_{CC10}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM Port Active t_{PC} (min.), t_{SCC} (min.)	80		100	mA	2, 3
			100		90		
			120		75		

DC CHARACTERISTICS (CONT.)

Parameter	Symbol	Conditions	Access Time	MSM51C262 Min.	MSM51C262 Max.	Unit	Notes
V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh and SAM Active	I_{CC11}	$\overline{RAS}$/$\overline{CAS}$ Cycling, SAM Port Active t_{RC}(min.), t_{SCC}(min.)	80		120	mA	2, 3
			100		100		
			120		85		
V_{CC} Supply Current, RAM/SAM Transfer Mode and SAM Active	I_{CC12}	$\overline{RAS}$/$\overline{CAS}$ Cycling, SAM Port Active t_{RC}(min.), t_{SCC}(min.)	80		125	mA	2, 3
			100		105		
			120		90		
V_{CC} Supply Current, Both Ports CMOS Standby	I_{CC13}	$\overline{RAS}$, $\overline{CAS}$, $\overline{SE}$, $\overline{WB}$/$\overline{WE}$, $\overline{DT}$/$\overline{OE}$ > V_{CC} − 0.5 V SC < 0.6 V	80		6	mA	
			100		6		
			120		6		
Input Low Voltage	V_{IL}			−1	0.8	V	
Input High Voltage	V_{IH}			2.4	VCC +1	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA			0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −2 mA		2.4		V	

AC CHARACTERISTICS (4, 5, 6)
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

(T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.)

Parameter	Symbol	-80		-10		-12		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Transition Time (Rise and Fall)	t_T	3	25	3	25	3	25	ns	
Refresh Interval (256 Cycles)	t_{RI}		4		4		4	ms	
Read or Write Cycle Time	t_{RC}	145		175		205		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	37K	100	37K	120	37K	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	55		65		75		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25		30		35		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		15		ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}	25	55	25	70	25	85	ns	7
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		20		20		ns	
$\overline{RAS}$ Hold Time	t_{RSH}	25		30		35		ns	
$\overline{DT}$ High Setup Time	t_{DHS}	0		0		0		ns	
$\overline{DT}$ High Hold Time	t_{DHH}	20		20		20		ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	60		70		80		ns	

AC CHARACTERISTICS (CONT.)

READ CYCLE

Parameter	Symbol	-80 Min.	-80 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit	Notes
$\overline{RAS}$ Access Time	t_{RAC}		80		100		120	ns	8, 9
$\overline{CAS}$ Access Time	t_{CAC}		25		30		35	ns	9,10, 11
Column Address Access Time	t_{CAA}		40		45		55	ns	9
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time RAS-Referenced	t_{RRH}	5		5		10		ns	12
Read Command Hold Time $\overline{CAS}$-Referenced	t_{RCH}	0		0		0		ns	12
$\overline{OE}$ Access Time	t_{OAC}		20		25		30	ns	9
$\overline{OE}$ or $\overline{CAS}$ to Output High-Z	t_{HZ}		20		25		30	ns	13
$\overline{OE}$ or $\overline{CAS}$ to Output Low-Z	t_{LZ}	0		0		0		ns	
Output Hold Time from $\overline{OE}$ or $\overline{CAS}$	t_{OH}	0		0		0		ns	

AC CHARACTERISTICS (CONT.)

WRITE CYCLE

Parameter	Symbol	-80 Min.	-80 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit	Notes
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		35		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25		30		35		ns	
Write Command Pulse Width	t_{WP}	15		20		25		ns	
Write Command Setup Time	t_{WCS}	0		0		0		ns	14
Write Command Hold Time	t_{WCH}	15		20		25		ns	
Data In Setup Time	t_{DS}	0		0		0		ns	
Data In Hold Time	t_{DH}	15		20		25		ns	
Write Mask Setup Time	t_{WBS}	0		0		0		ns	
Write Mask Hold Time	t_{WBH}	20		20		20		ns	
Write Mask Select Setup Time	t_{WS}	0		0		0		ns	
Write Mask Select Hold Time	t_{WH}	20		20		20		ns	
$\overline{OE}$ Hold Time Referenced to WE	t_{OEH}	10		10		15		ns	
Write Hold Time from $\overline{RAS}$	t_{WCR}	65		80		95		ns	
Data Hold Time from $\overline{RAS}$	t_{DHR}	65		80		95			

READ-MODIFY-WRITE CYCLE

Parameter	Symbol	-80 Min.	-80 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit	Notes
Read-Modify-Write Cycle Time	t_{RWC}	205		245		285		ns	
RMW Cycle $\overline{RAS}$ Pulse Width	t_{RRW}	140	37K	170	37K	200	37K	ns	
RMW Cycle $\overline{CAS}$ Pulse Width	t_{CRW}	85		100		115		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	110		135		160		ns	14
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	55		65		75		ns	14
Column Address to $\overline{WE}$ Delay	t_{AWD}	70		80		95		ns	
$\overline{OE}$ to Data In Delay Time	t_{OED}	20		25		30		ns	

AC CHARACTERISTICS (CONT.)

FAST PAGE MODE OPERATION

Parameter	Symbol	-80		-10		-12		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Page Mode Cycle Time	t_{PC}	55		60		70		ns	
$\overline{CAS}$ Precharge Time	t_{CP}	15		20		25		ns	
Access Time from Column Precharge	t_{CAP}		50		55		65	ns	15

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Parameter	Symbol	-80		-10		-12		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Setup Time	t_{CSR}	10		10		10		ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Hold Time	t_{CHR}	25		25		25		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{RPC}	0		0		0		ns	

AC CHARACTERISTICS (CONT.)

READ/WRITE, PSEUDO WRITE TRANSFER AND SERIAL READ/WRITE CYCLE

Parameter	Symbol	-80		-10		-12		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Serial Clock Cycle Time	t_{SCC}	30		35		40		ns	
SC Precharge Time	t_{SCL}	10		10		10		ns	
$\overline{SE}$ to Serial Out Setup Time	t_{SOO}	0		0		5		ns	
Serial Out Hold after SC High	t_{SOH}	0		0		5		ns	
Serial Output Access Time from SC	t_{SCA}		25		30		35	ns	16
Serial Output Access Time from $\overline{SE}$	t_{SOA}		20		25		30	ns	16
Serial Output Disable Time from $\overline{SE}$ High	t_{SOZ}		15		20		25	ns	13
SC Pulse Width	t_{SCH}	10		15		15		ns	
$\overline{SE}$ Pulse Width	t_{SOE}	10		10		10		ns	
$\overline{SE}$ Precharge Time	t_{SOP}	10		10		10		ns	
Transfer Command to $\overline{RAS}$ Setup Time	t_{DLS}	0		0		0		ns	
Transfer Command to $\overline{RAS}$ Hold Time	t_{RDH}	60		75		90		ns	
Transfer Command to $\overline{CAS}$ Hold Time	t_{CDH}	20		25		30		ns	
SC to Transfer Command Lead Time	t_{SDD}	10		15		20		ns	
SC Hold Time after $\overline{DT}$ High	t_{SDH}	10		10		10		ns	
Serial Data Input to $\overline{DT}$ High Delay Time	t_{SZS}		0		0		0	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	20		25		30		ns	
$\overline{DT}$ to $\overline{RAS}$ Precharge Time	t_{TRP}	65		75		85		ns	
Serial Write Enable Setup Time	t_{SWS}	10		10		10		ns	
Serial Write Enable Hold Time	t_{SWH}	10		15		20		ns	
Serial Write Disable Setup Time	t_{SWIS}	10		10		10		ns	
Serial Write Disable Hold Time	t_{SWIH}	10		15		20		ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	15		20		20		ns	

11

AC CHARACTERISTICS (CONT.)

READ/WRITE, PSEUDO WRITE TRANSFER AND SERIAL READ/WRITE CYCLE

Parameter	Symbol	-80		-10		-12		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Setup Time	t_{ES}	0		0		0		ns	
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	t_{EH}	20		20		20		ns	
Serial Data In Setup Time	t_{SIS}	0		0		0		ns	
Serial Data In Hold Time	t_{SIH}	10		10		10		ns	
SC to $\overline{DT}$ High Setup Time	t_{SDS}	0		0		0		ns	
SC to $\overline{RAS}$ Precharge Setup Time	t_{SCR}	0		0		0		ns	

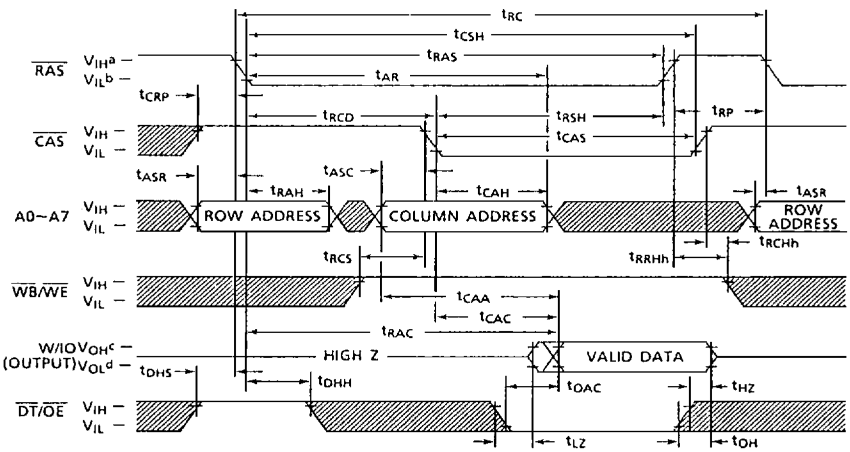
Notes:

1. An initial pause of 200 μs is required after power-up followed by a minimum of any 8 $\overline{RAS}$ cycles (example: $\overline{RAS}$-only Refresh) and SC cycles of greater than 8 cycles before proper device operation is achieved.
2. I_{CC} current depends on the output loading when the output is enabled. ICC (max) is measured with all output open.
3. I_{CC} current depends on the number of address transitions with $\overline{CAS}$ held at the V_{IH} level. The spec. I_{CC} (max) is measured using a maximum of two transitions per address input for each random access cycle and one address change for each Fast Page mode cycle.
4. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.
5. If clocks are stopped beyond the maximum refresh period of 4 ms a pause of 200 μs followed by a minimum of any 8 $\overline{RAS}$ cycles (example: $\overline{RAS}$-only Refresh) is required before proper device operation is achieved.
6. The AC measurements assume the transition time (t_T) = 5 ns. All AC measurements are made with V_{IL} (min.) > V_{SS} and V_{IH} (max) < V_{CC} and using a load circuit equivalent of 2 TTL loads with either 50 pF or 100 pF in parallel.
7. The spec. t_{RCD} (max.) is for reference only. The spec t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.)
8. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for refrence only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, the access time is controlled exclusively by t_{CAC}.

9. Measured using an equivalent load circuit of 2 TTL loads and 100pF.
10. The measurement assumes $t_{RCD} > t_{RCD}$ (max.).
11. Access time is defined by t_{CAA} rather than t_{CAC} if $t_{ASC} < (t_{CAA}$ (max.) – t_{CAC} (max.) – $t_T)$.

TIMING CHART

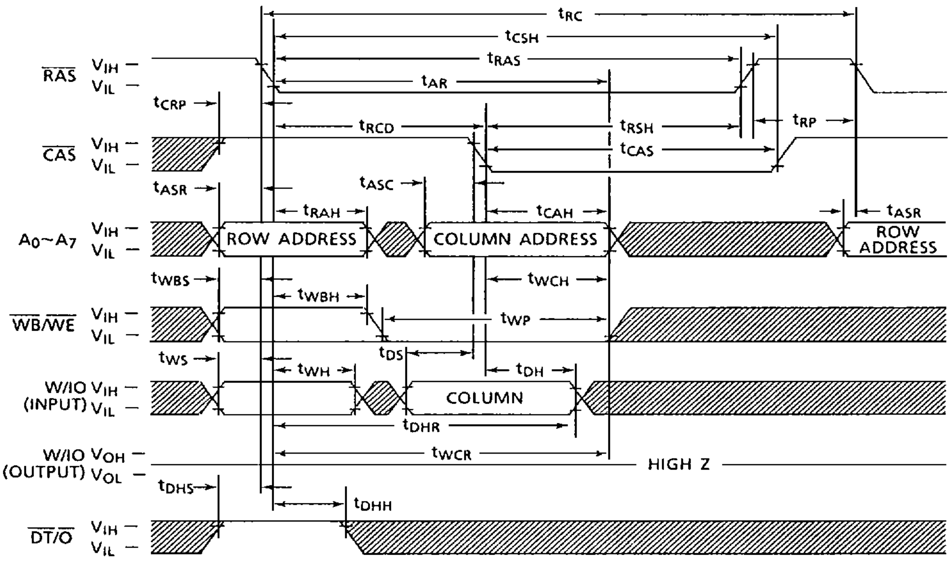
READ CYCLE



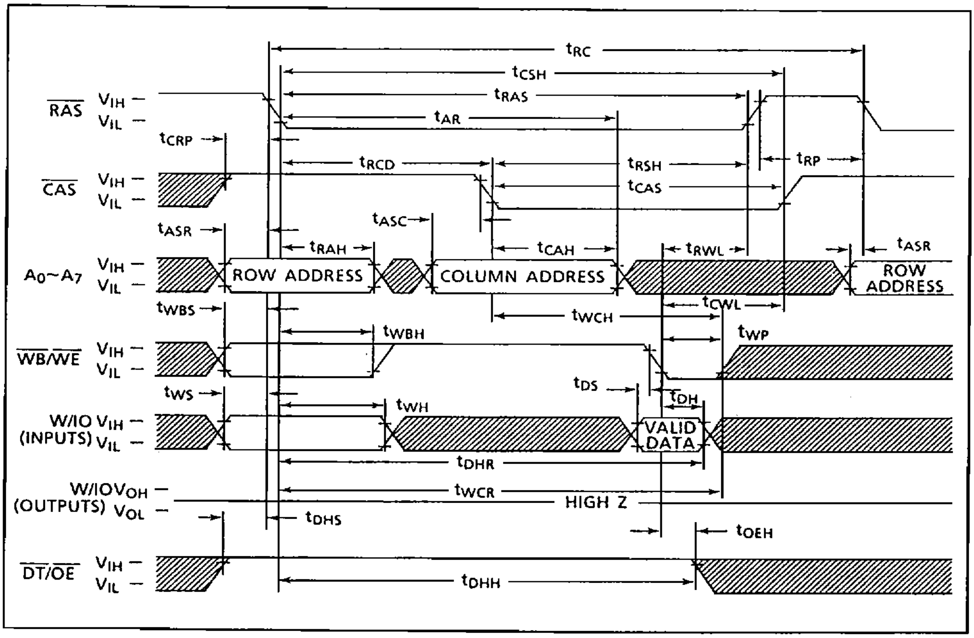
Notes:

a, b: V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
c, d: V_{OH} (min.) and V_{OL} (max.) are reference levels for measuring timing of D_{OUT}.
e: t_{LZ} is referenced to the lesser of $\overline{CAS}$, and $\overline{OE}$ low transition.
f: t_{HZ} and t_{OH} are referenced to one earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.
g: Transition is measured + 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
h: Either t_{RCH} or t_{RRH} must be specified.

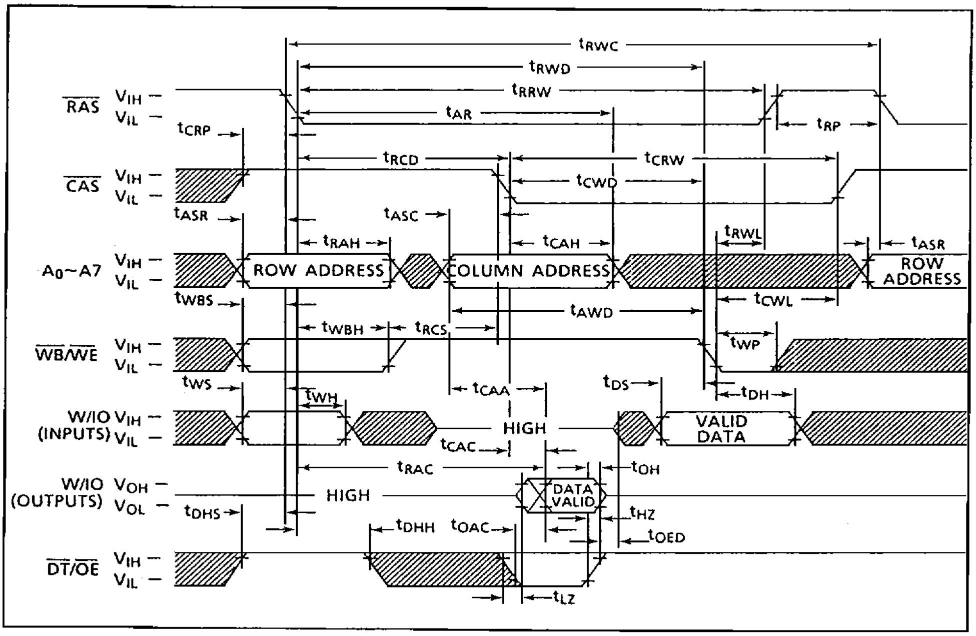
WRITE CYCLE (EARLY WRITE)



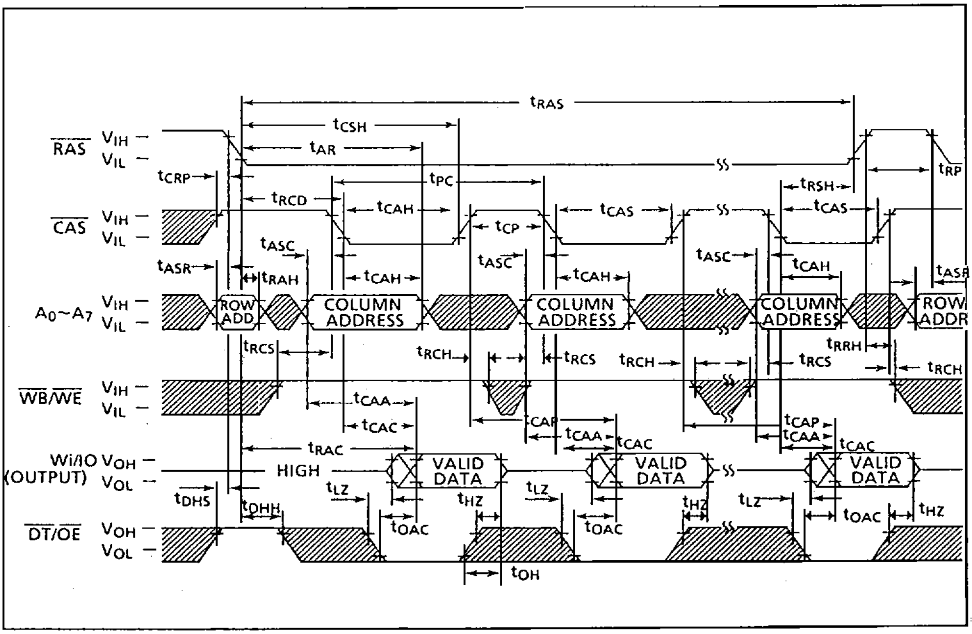
WRITE CYCLE (DELAYED WRITE)



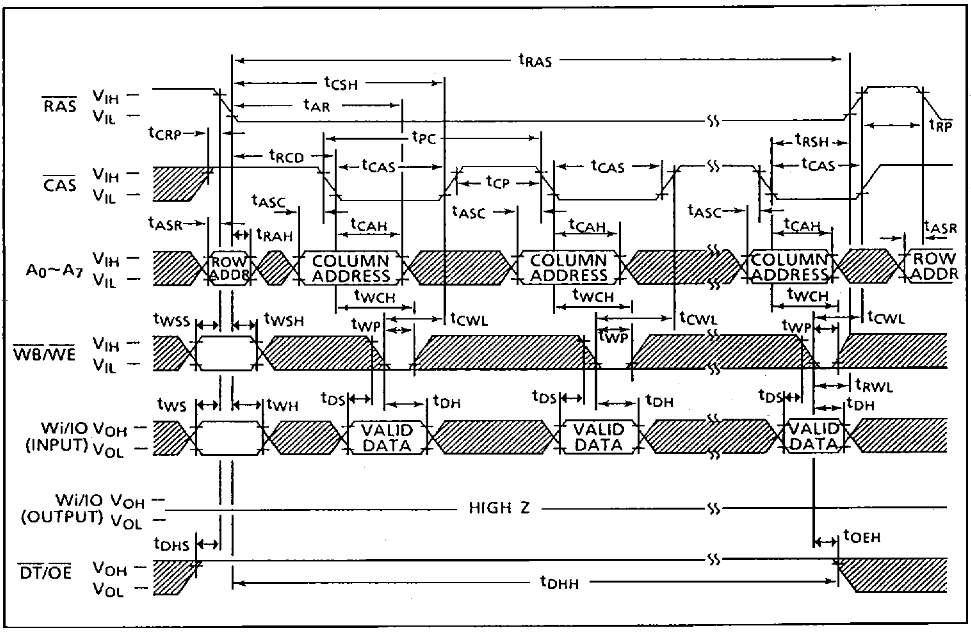
READ-MODIFY-WRITE CYCLE



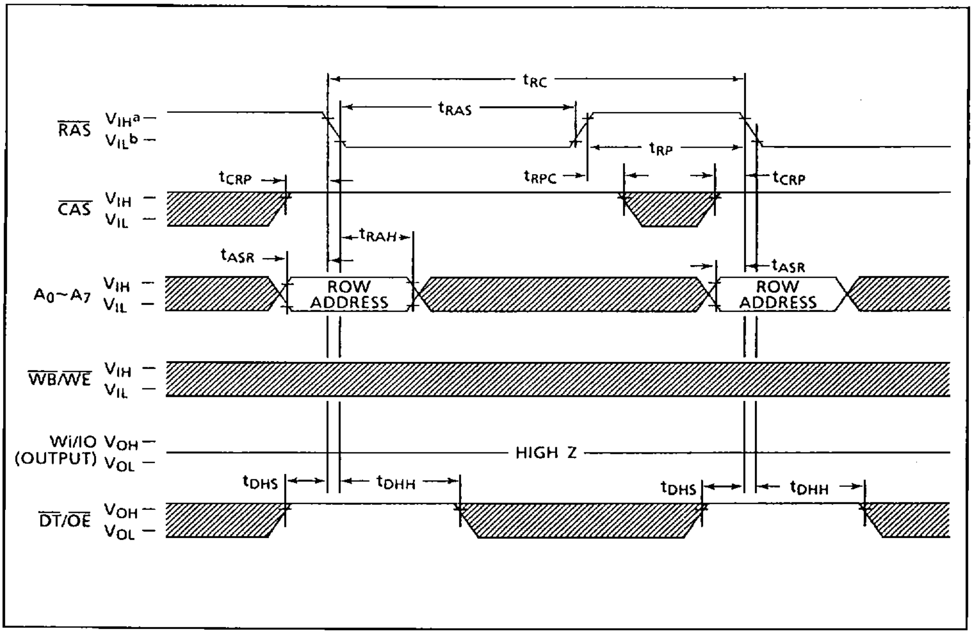
WAVEFORMS OF FAST PAGE READ CYCLE



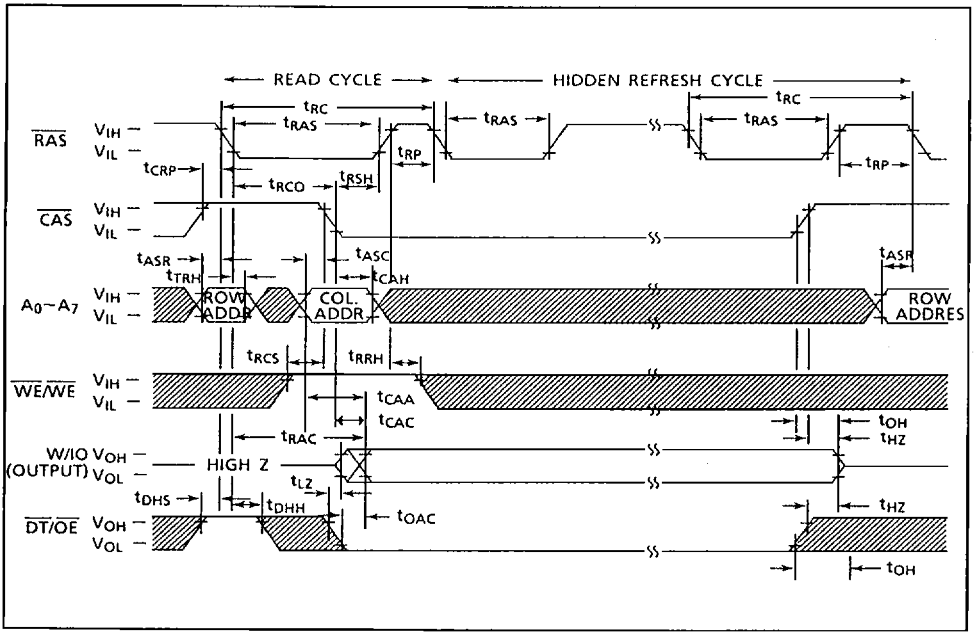
WAVEFORMS OF FAST PAGE MODE WRITE CYCLE



RAS-ONLY REFRESH CYCLE

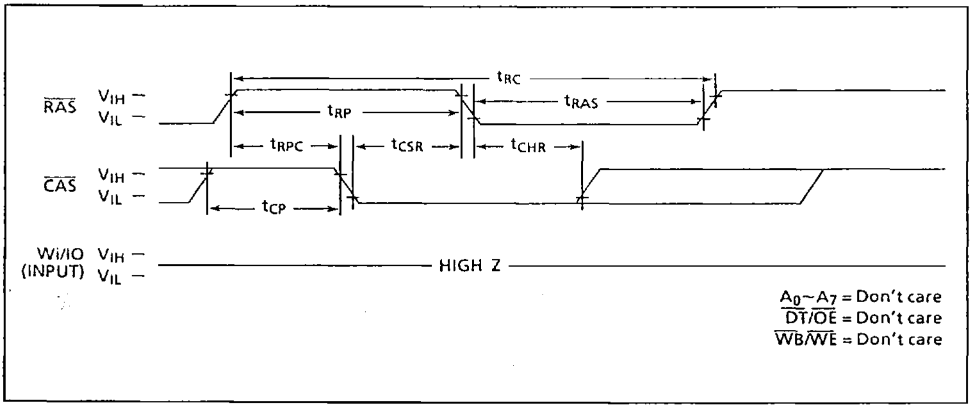


HIDDEN REFRESH CYCLE

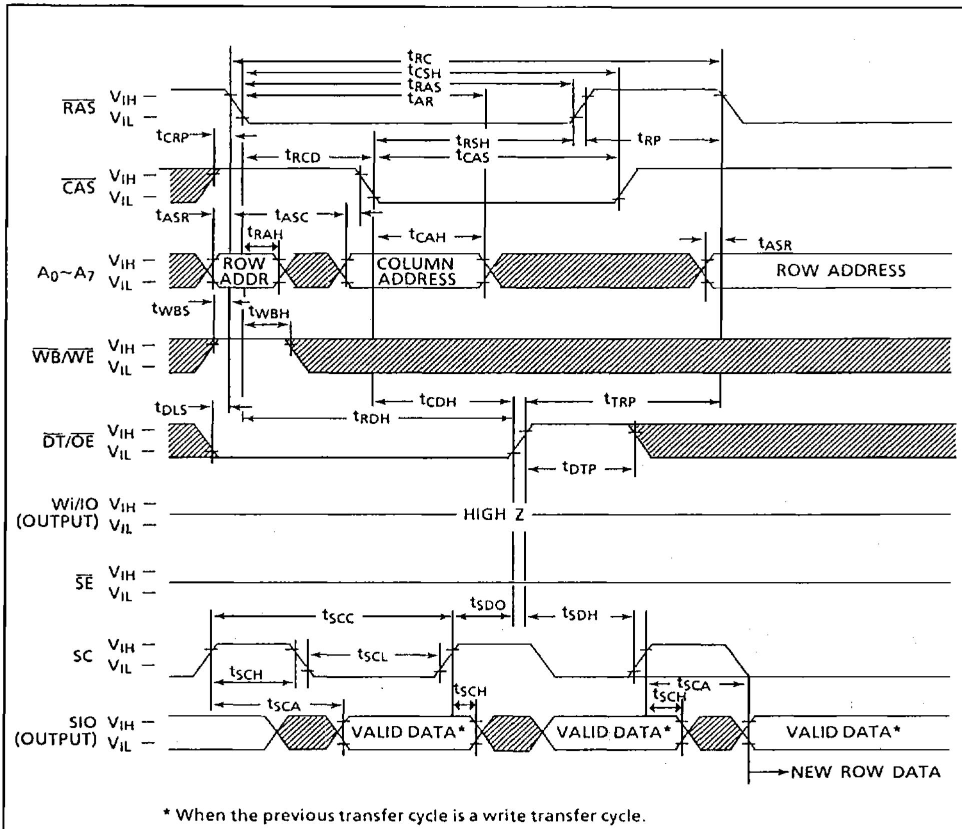


11

CAS BEFORE RAS REFRESH CYCLE

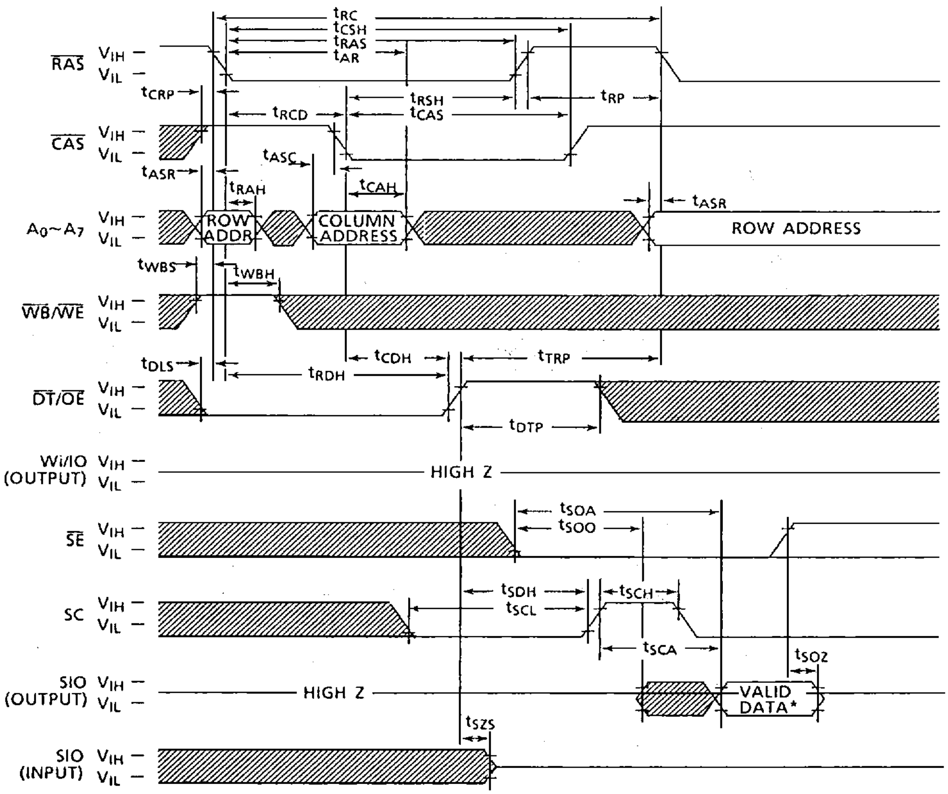


READ TRANSFER CYCLE (RAM → SAM) SERIAL READ SETUP*



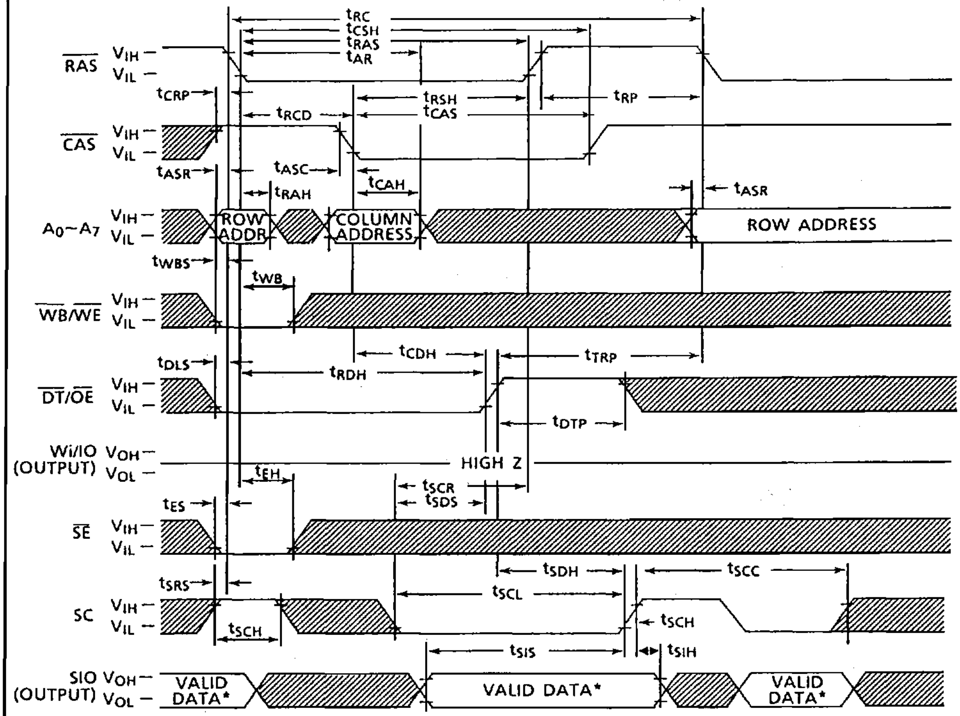
* When the previous transfer cycle is a write transfer cycle.

READ TRANSFER CYCLE (RAM → SAM)



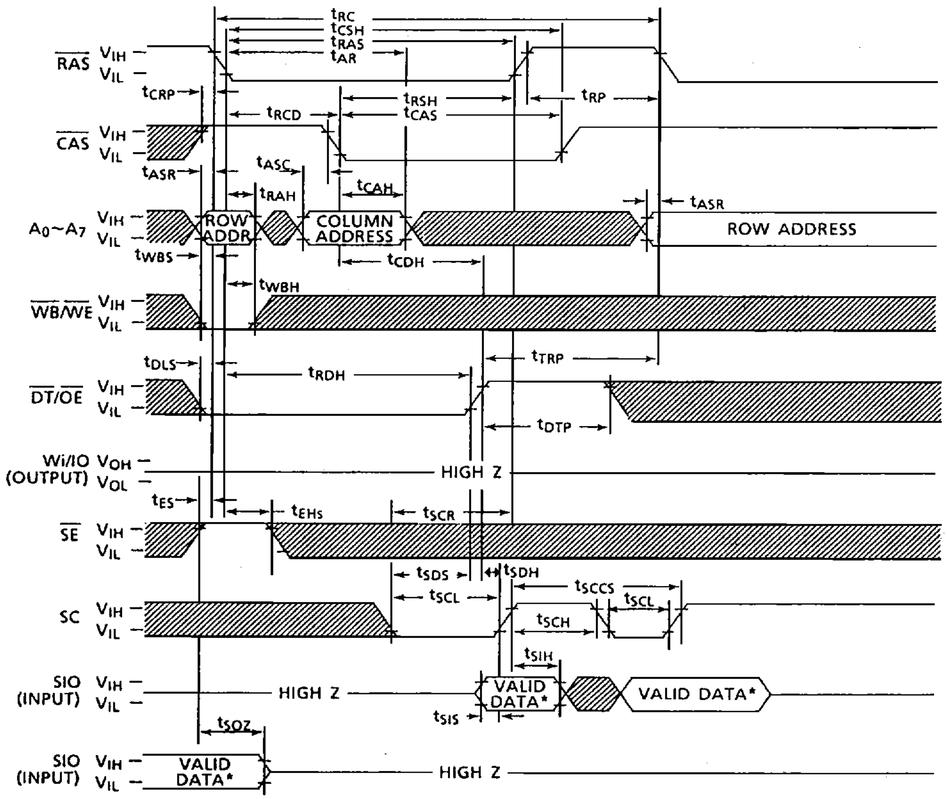
* When the previous transfer cycle is a write transfer cycle.

WRITE TRANSFER CYCLE (SAM → RAM)



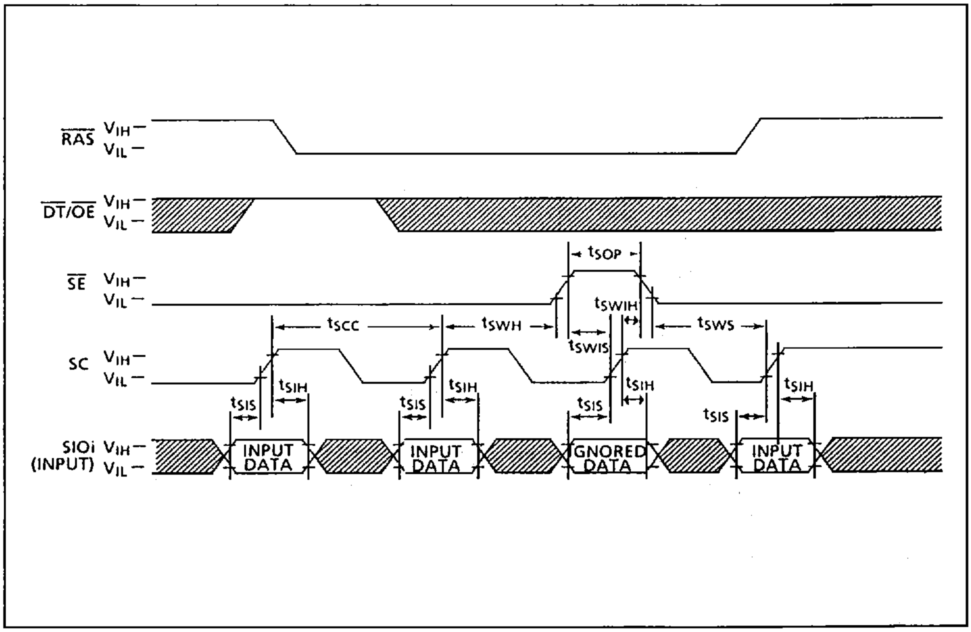
* NOTE: If SE is "H" level, the serial input data is not written into the data register, but the serial data selector continues to function.

PSEUDO WRITE TRANSFER CYCLE SERIAL WRITE SETUP

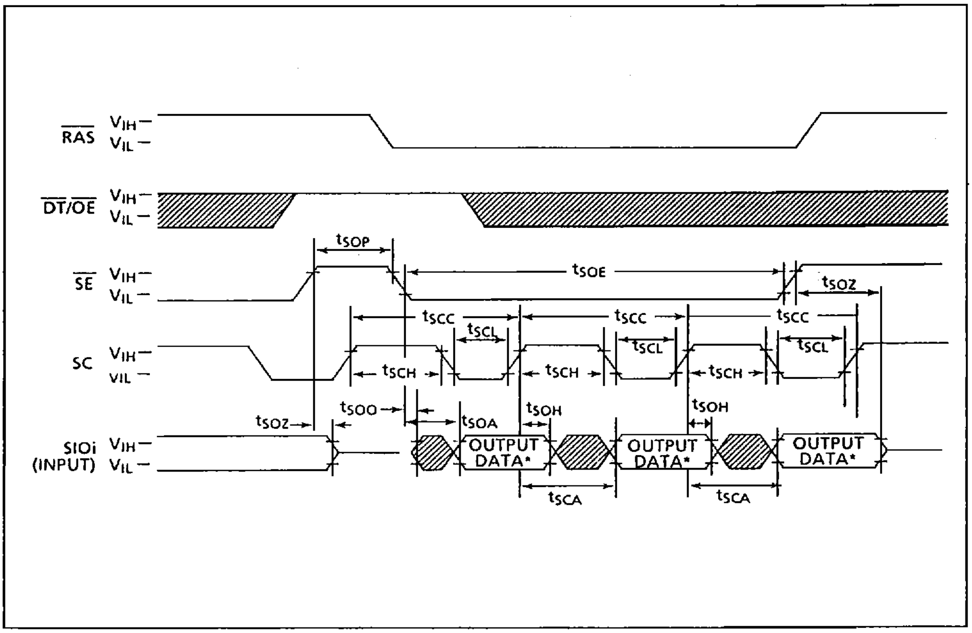


* NOTE: If $\overline{SE}$ is "H" level the serial input data are not written into the data register, but the serial data selector is worked.

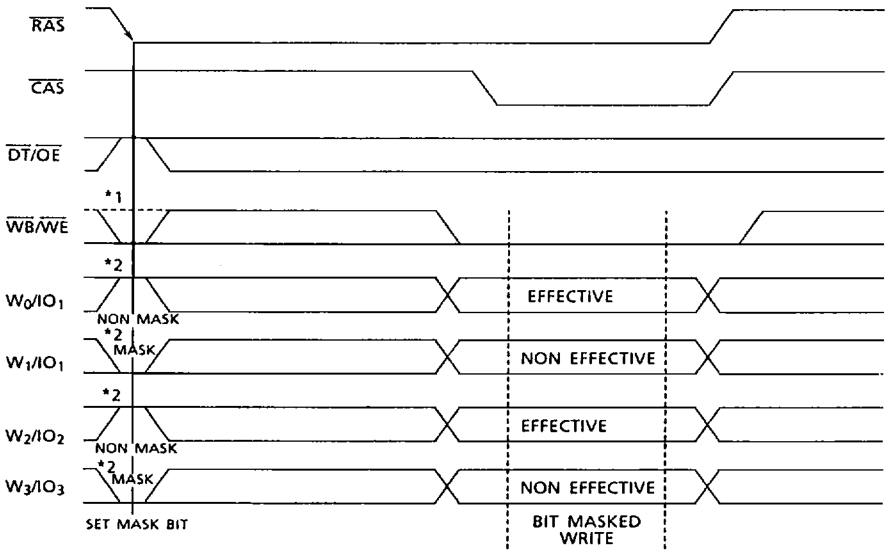
SERIAL WRITE CYCLE



SERIAL READ CYCLE



BIT MASKED WRITE

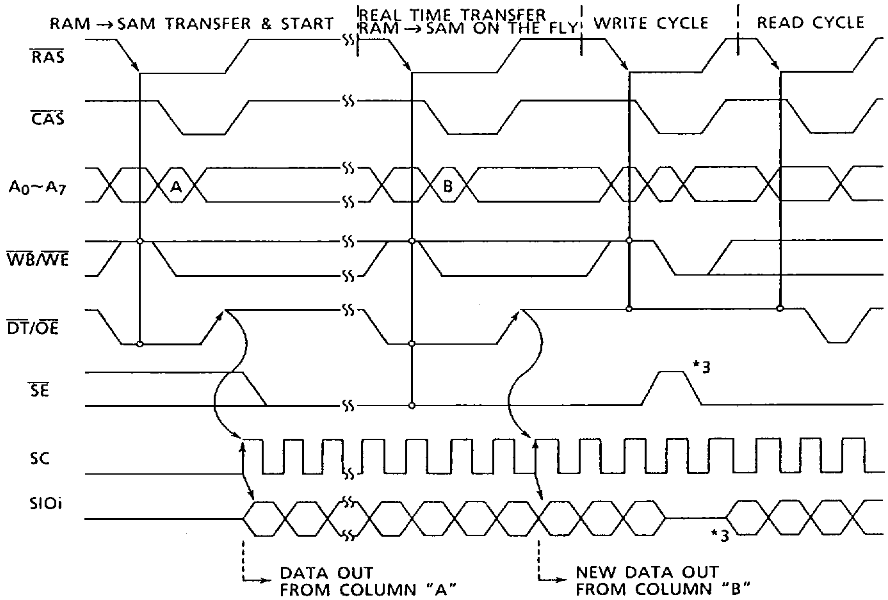


*1 If $\overline{WB}/\overline{WE}$ = "H" all 4 bits of data are written into RAM

*2 $W_{0\sim3}/IO_{0\sim3}$ = "H" Nonmasked
$W_{0\sim3}/IO_{0\sim3}$ = "L" Masked

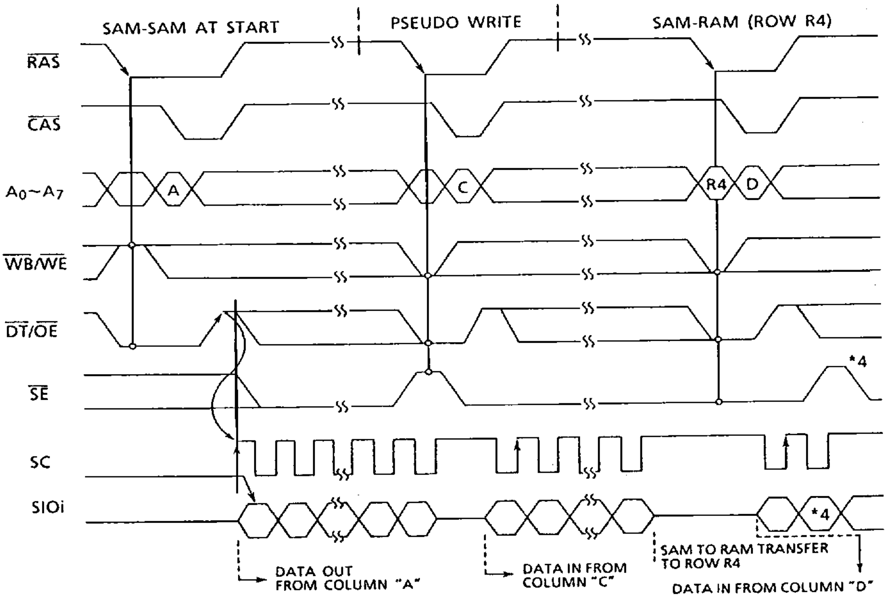
11

SERIAL OUTPUT MODE



*3 If $\overline{SE}$ goes to "H" level, SIOi enters the high impedance state, but the serial data selector continues to function.

SERIAL INPUT MODE



*4 If $\overline{SE}$ goes to "H" level, SIOi input data is ignored, but the serial data selector continues to function.

11

FUNCTIONAL DESCRIPTION

RAM Operation

The MSM51C262 is a CMOS dynamic memory with 2 ports. One port, the RAM port, operates in the same way as the 64K x 4 DRAM. The other port, the serial access port (SAM), allows data to be either read from or written to the memory at very high data rates.

The MSM51C262 reads and writes data via the RAM port by multiplexing a 16-bit address into an 8-bit row and an 8-bit column address. The row address strobe ($\overline{RAS}$) latches the row address on the chip. The column address, however, flows through the internal column address buffer and is latched by the column address strobe ($\overline{CAS}$) signal. Because column access time becomes primarily dependent upon a valid column address rather than the falling edge of $\overline{CAS}$, signal timing restrictions on $\overline{CAS}$ can be greatly loosened with no effect on access time.

Memory Cycle

A memory cycle is initiated by the falling edge of $\overline{RAS}$. A memory cycle cannot be ended or cancelled prior to fulfilling the t_{RAS} (min.) timing specification once it starts. This precaution is necessary for proper device operation and integrity. A new memory cycle cannot be started until the minimum precharge time t_{RP}/t_{CP} is satisfied.

Read Cycle

A read cycle is a memory cycle in which data is retrieved from the memory array and presented on the Wi/IOi pins. Read cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Write Cycle

A write cycle is a memory cycle in which data supplied externally to Wi/IOi is written into the location in memory specified by the address. Using the masked write function, any combination of Wi/IOi lines can be written and the remainder ignored. Write cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Refresh Cycle

To retain the data in a MSM51C262 DRAM, a refresh operation activating each of the 256 row addresses must be performed at least once every 4 ms. Any operation such as read, write, RMW, $\overline{RAS}$-only cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, or transfer cycle refreshes the addressed row.

Fast Page Mode Operation

Fast Page Mode permits an 256 columns of 4 bits within a selected row of the MSM51C262 to be randomly accessed at a high data rate. After a normal cycle initiation, maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to resupply it. The column buffer acts as a transparent latch data while $\overline{CAS}$ is high and, when $\overline{CAS}$ goes low, holds the addresses applied. Because of the transparent latches, the column address flows through and the read access begins upon stable addresses rather than the falling $\overline{CAS}$ edge. This eliminates t_{ASC} and t_T from the critical timing path and helps to speed up access while making operation simpler.

During a Fast Page Mode operation, read, write, read-modify-write, or read write-read cycles are possible to random addresses within a selected row. Multiple operations to the same address are permitted as well as more than 256 accesses to any combination of addresses within the selected row. The only limiting factor to the number of such Page Mode accesses is refresh timing. Following the entry cycle into Page Mode, access time is t_{CAA} or t_{CAP}-dependent. If the column address is valid before or coincident with the rising edge of $\overline{CAS}$, t_{CAP} is the access controlling parameter. If the column address is valid after the rising edge of $\overline{CAS}$, access time is determined by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output buffers.

With Fast Page Mode, very high sustained data rates can be achieved. The following equation can be used to calculate the data rate possible:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255t_{PC}}$$

11

MODE SELECTION

RAM Operation to be Performed	SAM Mode to be Entered	AControl Signals (Sampled at the falling edge of $\overline{RAS}$)					$A_0 \sim A_7$ Sample Time	
		$\overline{CAS}$	$\overline{DT}$/ $\overline{OE}$	$\overline{WB}$/ $\overline{WE}$	$\overline{SE}$	W/ $IO_{0 \sim 3}$	$\overline{RAS}$	$\overline{CAS}$
Read	Mode not affected			X	X	X	Row	Column Add.
Write	Mode not affected		H	H	X	X	Row	Column Add.
Bit Masked Write	Mode not affected			L	X	H*	Row	Column Add.
	Mode not affected	H		L	X	L*	Row	Column Add.
RAM → SAM Transfer	Output Mode			H	X	X	Row	SAM Start**
SAM → RAM Transfer	Input Mode		L	L	L	X	Row	SAM Start**
Pseudo Transfer	Input Mode			L	H	X	X	SAM Start**
$\overline{CAS}$-before-$\overline{RAS}$ or Hidden Refresh	Mode not affected	L	X	X	X	X	X	X

X = Don't care

* The state of the W/IO lines is sampled at the falling edge of $\overline{RAS}$ to set the Write Bit Mask Register. If W/IO is high at the falling edge of $\overline{RAS}$, no masking action is taken and the corresponding data bit is subject to change by a write operation. If W/IO is low at the falling edge of $\overline{RAS}$, the corresponding bit is masked and is not altered by a write operation.

** The 8 address signals, A_0 to A_7, are used to select the RAM row address that is affected by a transfer to or from the SAM, and the starting address for a SAM read or write operation. The falling edge of $\overline{RAS}$ strobes the row address, and the falling edge of $\overline{CAS}$ strobes the SAM starting address.

COMBINED RAM-SAM OPERATION

Transfer

The transfer operation of the MSM51C262 allows a row (256 bits) of data to be transferred between RAM and SAM in either direction. The signals and states that control the transfer operation are specified in the Mode Selection Table.

To start a serial write operation, it is necessary to cause the SIO_0 to SIO_3 pins of the SAM, port to be in a high-Z state. The pseudo write transfer cycle accomplishes this and must be performed any time the SAM mode is to be changed from read to write. No data transfer takes place, but addresses are set up as in any other transfer cycle. A read transfer cycle (RAM to SAM) changes the mode from write to read.

SAM OPERATION

SAM is organized as 256 words x 4 bits per word. SAM can be loaded from two sources: RAM and the external serial I/O lines, SIOi. SAM has two operational modes, read and write (viewed externally). Mode changes are described in the previous section.

When SAM is in read mode, data is first transferred from RAM to SAM and then can be accessed serially via the SIOi lines, beginning with any SAM address. The progression of data output is from lower to higher numbered bits and addresses are module 256.

When SAM is in write mode, data is captured in SAM by using the SIOi lines, and can be written into a selected row in the RAM by a write transfer operation.

Read/Write

The SC pin is used as a shift clock for the SAM port. Serial access is triggered by the rising edge of SC. When SAM is in write mode, the rising edge of SC causes data to be strobed into the selected SAM cell. In the read cycle, output data becomes valid after t_{SCA} from the rising edge of SC and remains valid until the next cycle. The SAM address is automatically incremented by SC.

The $\overline{SE}$ pin is used as an output/input enable pin for the SAM. It does not, however, gate the SC signal, and the SAM address counter for read or write operations continues to increment regardless of the state of $\overline{SE}$.

11

Real-time Read Transfer

The MSM51C262 offers real-time read transfer between RAM and SAM. By using this feature, a continuous data stream can be generated even if the row address must be changed. No loss of timing is caused by this transfer. The data transfer from the RAM to SAM is triggered by the rising edge of DT/OE after the RAS/CAS cycle sets up the data to be transferred and the start address. New row data is available for SAM output after $\overline{DT}/\overline{OE}$ returns to a high state in compliance with specification parameters t_{SDD} and t_{SDH}. SC should be applied continuously and $\overline{DT}/\overline{OE}$ timed from SC to achieve non-stop transfer.

Write Transfer

After SAM is placed in write mode and the required data is captured via SIOi, the write transfer operation causes the SAM content to be written into the selected RAM row. After the write transfer cycle is completed, more data can be written to SAM via SIOi.

Power On

After application of the V_{CC} supply, an initial pause of 200 μs is required followed by a minimum of 8 initialization $\overline{RAS}$ cycles (any combination of cycles containing a $\overline{RAS}$ clock) and minimum of 8 initialization SC cycles. 8 initialization cycles are required after extended periods of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified refresh interval. During Power On, the V_{CC} current requirement of the MSM51C262 depends on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during Power On, the device goes into an active cycle, and I_{CC} exhibits current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power On to avoid current surges.

SIOi after application of the power supply is initialized in the input mode, but this state can not be guaranteed because of the control signal level during power On. Therefore, after V_{CC} reaches the specified voltage with power On, we recommend to be initialized after carrying out 8 initialization cycles after 200 μs.