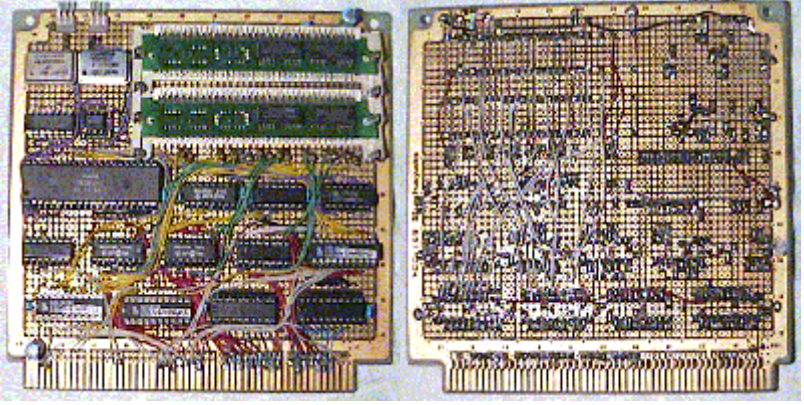

# Production of 10M RAM boards X680x0

## Introduction

I mean I think, and I want to make the board as an external memory for X68, with the SIMM 30pin. In circuit is identical to that of Mr. Okuyama actually flowing in the streets. Have you ever been also published transistor technology. In recent years, it has been released I say "XSIMM10", also board the same function at all. We think in that sense, but may not be worth much, and interesting to try making is also the study of hardware.
Is "a little bit of knowledge and patience" as the secret of success. I think I might be able to somehow even better amateur. Is in the form of machine clock also supports up once. Is operating in any NoWait (17MHz) EXPERT me.

## Schematic

. It is a PS file. Please take down. I am not confusing the following discussion that there is no circuit diagram.
Circuit diagram is here

## Price to be worried about

7000 yen total + α

In the price is, I think This is the way it goes. Please note that price does not contain the SIMM. Seems to be good in about 80ns access time SIMM. Parity may or may not. I am fully implemented in about 20000 yen all inclusive hopefully. I became cheaper memory.

## Parity bit

The parity bit that is a bit for the sign in error and remember if there is an even number or an odd number of bytes in a single High. The communication is something I will come out well. It does have this parity for the IBM / PC, is not for the Mac. I think this time we will not use this bit, but I think there is no good and if anything, with nothing to do so separately.

## Material considerations

The substrate for the X68, is not to enter the hand too much now. It may not get Nihonbashi, Osaka, and not side Ri Akihabara, Tokyo. Kyoritsu of Osaka electrons

are like mail order is doing well, I would be close to those who do not have any parts store to try to contact us.
Diagonal SIMM socket is a type of two minutes was together. If you have a spare slot, such as PRO is probably the socket may be vertical. Towards the vertical, but is a bit cheaper, the slot occupied two minutes.
It is IC, I can be a thing of the F type AS type stuff. 158 I 157 also does not matter. 74ALS04 would probably be okay but 74LS04. I can be a 7407 74LS07.
This board is using GAL. It will be referred to as cowardice, but what will be said, I use the GAL. In the parts shop in Akihabara that T-ZONE is like is doing (surcharge) write GAL.
Although resistance, please be prepared about 20. Should be good in tens of Ω resistance. I think I set resistance, and may be between 3.3k ~ 10k.
I think there are also about twenty multilayer capacitor. I hope there was one about two electrolytic capacitors. IC socket is, I think you need about amateur. I'm using the IC socket all the time. There can be any guy round pin high Bundy also made cheap, but I still have the higher excellent in many ways. However, please note that there is a high probability than IC. GAL is just me but I may be in the round pin.

## First stage

I want to wire the power supply and GND first. Array of card edge side of X68, so listed in the instruction manual of the X68, please refer to that. Kyoritsu Electronic board I bought in, because with the power supply and GND pattern is less than the show you around the circumference of the board, you can easily wire. The location of the pins on the SIMM, are as follows.

| One | Two | Three | Four | Five | Six | Seven | Eight | Nine | Ten | Eleven | Twelve | 13 | 14 | Fifteen |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VCC | CAS | DQ0 | A0 | A1 | DQ1 | A2 | A3 | GND | DQ2 | A4 | A5 | DQ3 | A6 | A7 |
| Sixteen | 17 | Eighteen | 19 | Twenty | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | Thirty |
| DQ4 | A8 | A9 | A10 | DQ5 | WE | GND | DQ6 | NC | DQ7 | Q8 | RAS | CA8 | D8 | VCC |

VCC is the power of that. Q8 CA8 D8 of the second half of that is pin for parity. This is intended 4MSIMM, No. 19 is in the NC in 1MSIMM. It means that the NC is an abbreviation for NonConect, that it does not cost anything. The opposite of the power IC pin 1, GND is pin on the end of the diagonal.
Now that you have finished wiring · GND power, install a bypass capacitor (bypass capacitor for short). Install a capacitor between the GND and the power source, such as IC, this is something to reduce the noise. Capacitors are not direct current. However, when you change the potential of the power supply · GND due to noise, the capacitor has become a mechanism to absorb the change. It is working like a cushion. · GND power supply based on a large, you may wish to install the electrolytic capacitor might be good. The electrolytic capacitor, please note that there is a pair of field polarity and 圧限. Please install what is the notation - towards GND, "". I think I versus pressure, and may be about 6.3V. Capacity with 330μF. If the wiring is done up there, please make sure the power supply and GND are shorted or not in the tester. More specifically, I put a pin on the power supply and GND to the resistance range. On the relationship you have with the capacitor, the needle swings moment. It is OK if the resistance value becomes almost infinite. But please be careful if you've

soldered directly to the IC socket with no resistance will not be infinite. I think in this case, the resistance value should be 0.

## Second step

All that is left is to wiring schematic street. In this case, the address of the SIMM · CAS · RAS · WE, please wire the resistor between the signal line and the pins in the socket. What is called the damping resistor, this is, except for the one under noise and etc.. If many chips have been previously connected to the signal line, the called under-and-over means that the noise can be very large when the signal change.
If the SIMM, the above signal line, the chip also has eight signal wires hanging from the tip of the case of 8 chips. Chip if the data line is taking because it is one, it is not necessary to install. However, the resistance increases, the propagation delay of the signal appears. Well, it would be okay if Ω but dozens. Let me set the data bus pull-up resistor. I do not have to be without. Mounting position, it does not matter between SIMM and 74AS245.
Wiring has been completed, I will check the wiring one by one. In addition to wiring, through next line if there are any such, I'll keep checking may not be short-circuited with the power supply and GND. The reason for this is that you have three to two times a check would be good. Please completely eliminating disconnection, and poor soldering. If you fail to do this, is very difficult to debug later.

## Pull-up

And pull-up means that the power supply connected (through a resistor) signals. Why I say through the resistance in the middle, when (0V), the signal would short-circuit the power supply and GND there is no Low level resistance. I mean you have a resistance to avoid it. In this resistor current is constantly flowing a little while. I am able to supply a current of something weak signal, changed to a strong signal for that. Also, if you want to fix the signal High, but to direct the power Expo emblem, sometimes ON · OFF the main power source, it may take a voltage higher than the specified voltage. Sometimes for such occasions, you put a resistor.

## The role of each IC

74AS245 is a so-called bus buffer. In the tri-state output, I serve to connect the content of the data off or Dari bus on the board body. It also includes the expansion board for what I (but of course). Say why, it is because the data on the data bus is in trouble strikes. It is very dangerous even though the data is coming from the I / O of the body, the data of the RAM on the board and ride to the data bus of the body. There may be a break element is hit output.
74AS158 is used to select the address. I want to output two signals one by one. Because it is a specification of the DRAM, which will be described later.
74ALS04 are used to generate timing. with the amount of time that the signal passes through the 04, I'm making the timing. It is an example of a bad considerably. I dont have to use the delay element with a decent really, I was here as easily choose.
Used only for signal DTACK, 74LS07 is an open-collector output buffer. This is the signal itself does not change. DTACK signal is bad and so direct connect, I'm across the 07 in between.
It is GAL, one is using the address decode. I have decided from the top of the address

bus, whether or not you want to access the SIMM. One is making a signal, such as for various other SIMM. Some of these might be 4-5 in the individual normal TTL, you need one in the GAL.

## Buffer

I said something to the role of the inverter NOT to reverse buffer, the contents of the signal and outputs the signal without changing the content. Also output state, and the like (3-STATE) · Open-collector Three State also totem pole.

## GAL programming

In this board, to create various signals using the GAL.
The GAL first, we use the address decoded using the top of the address bus. We make a signal RAM2 to access towards the SIMM_2 and it between $ A00000 ~ $ BFFFFF, the signal RAM1 to access towards the SIMM_1 address is it between $ 200000 ~ $ 9FFFFF. By changing this part, can be changed to any four pieces 1MSIMM.
In one GAL, is generating an address signal and a signal selector for SIMM, DTACK, such as refresh anymore.
The list of programs that GAL is to JEDEC file by a file that was written to make it easier for humans to program a GAL, and then compile it. If you burn the GAL, JEDEC file has become fundamental. By going to a place that will burn with this file to get the desired burn GAL. Equivalent circuit diagram, it is shown at all positive logic. It would be very hard to see that it is a person skilled in hard, please forgive me.
(. PS) and an equivalent circuit here JEDEC file for GAL

## RAM

General types There are two kinds of RAM (Static) RAM D S and (Dynamic) RAM broadly. I have been able to in the transistor SRAM, DRAM charge is rapidly lost and left alone because they can be a capacitor, the content is lost. DRAM, you must not be carried out without having to re-write operations on a regular basis which is said to be refreshed for this purpose.
SRAM who do not need a refresh. , But because it does not go up too much accumulation rate calorific expensive than DRAM, in the mass memory using a DRAM. In favor of the SRAM is capable of high-speed access, are also used as cache memory, however.

## DRAM and access methods of signal

Requires various signals in DRAM. This is due to how to access the DRAM, there is no way.
Behavior is good reason to access the RAM is that it gives the address written to receive data, or data.
Address line is not only half the number of pins that are used for the DRAM. If one bit, it is not only the address lines to the 9-bit DRAM 256k (32k bytes) is output. Now, as to whether to pass address how, I would split into two address. This is how to give the address with which you can access within a DRAM is built to break up the Row and Column. If you think of to say Column square matrix memory space is equivalent

to Row row row. If you give the address of the DRAM address at Row, it signals that tell the DRAM Row address of the address of the RAS and now says (RowAddressStrobe). Culumn address signal, and to teach it says and CAS (ColumnAddressStrobe). The order in which the address is given away towards the Row address is determined. 're A role switch this address, select the address IC, at this time I use it as a 74AS158.
Output to the DRAM address lines of the 1 · Row address and write access methods when reading.
(To activate the RAS) indicating that the address is out in Row 2 · DRAM.
Output to the DRAM address lines of the 3 · Column address.
(To activate the CAS) indicating that the address is out in Column 4 · DRAM.
5 Remove the data.
To non-active 6 · RAS CAS.
(There is also a bad RAM is CAS and change period) that captures and DRAM address, which you can then change the address at the moment of RAS CAS becomes active, so captured. As a signal to tell the current state of a read, or a write, there is a (WriteEnable) WE. At the time of writing, it is active at the time of reading has become when it is not. There are two modes of writing to DRAM. This time I use a thing called EarlyWrite. This is how you activate the WE before giving the address. Some say DelaiedWrite is issued after a CAS to WE.
How to give the address is the same as when reading. When the CAS is activated, data is captured in DRAM.

## Refresh

Contents will be lost if you leave them alone DRAM is as described above. I'll not to refresh at regular intervals, I will not be there.
This guy is very tedious, but I can not refresh in CPU even if you want to access the memory. This time, I'm using the body as a refresh signal is issued. time a refresh is required is different for each DRAM, likely because of the body for a minimum, I think it's okay.
I have a refresh too kind, I take this method is that CAS Before RAS. This is when you want to access normally, I activate ahead towards the RAS, refresh completed by DRAM and things to do to enter the refresh mode freely by yourself when you activate before the CAS, lowering the RAS to. So, it is possible to perform an external signal, you only have to activate the RAS and CAS. Address does not matter at this time.
RAS Only refresh the old saying, I was just a way to activate the RAS Row address circuit giving. And it is this, You will have to perform a refresh by changing all the Row address. I do not refresh me only at the Row address and only once. The CAS Before RAS, all without asking me for DRAM has a counter inside. Row address has come out in order for the refresh (instruction decode cycle) M1 cycle in the Z80. Contained in the R register is also its contents.

## X68 signal

I do not do not do it around with the control signal from the body even if it says make a simple board RAM.
Address bus and the data bus is the data path and address as its name suggests. In the peripheral 68k inform the content of its data and address and are currently riding on

the bus, but he is a signal (LowerDataStrobe) (UpperDataStrobe) · LDS (AddressStrobe) · UDS AS.
(Although it is so word), 68k is not A0 of address (2 bytes), so that the underlying word access. So, the minimum access unit becomes one word. If you want to read and write only one byte, you have realized by controlling the signal of UDS LDS.
Tell a 68k signal DTACK and that it is ready for data passed, or that I was able to receive the data surrounding I (DataTransferACKnowledge). 68k is I have been fundamental period 4 clocks (around does not return) DTACK that this does not become active until the third clock, 68k is wait around is to or make or receive data. This is a guy that contain so-called wait.
It is slow and memory, it takes time until you have determined the data, I put a wait in this state. However, DTACK is not returned matter how much time passes, would cause a bus error is 68k. I must not return a DTACK not really like this, and is ready for data, this time on the board of such a thing, we'll return to anyway. I work in any case NoWait This way, I will read and write the contents of a completely different side of a slow memory. I should not because it does not happens, and not to read or write data on the board firmly.
Refresh-related signals are used as a signal that the unit is used for the main memory in this board. INH2 signal that is the signal seems to be out when you are refreshing the body memory.

## Access Timing

There in order to access the DRAM, that's a very important factor in timing. This is preventing the general public to connect the DRAM. I think we would like to describe using a very simple timing table.
First, RAS is activated on the propagation delay of one minute GAL from the falling edge of AS. We will assume this is the GAL to use so that the maximum delay of 25ns, and the late 15ns. RAS-CAS delay time refers to the time between the CAS from the RAS, and the time required tens of ns. Also, I will change the address in the meantime. RAS-CAS delay time to generate this, we create a three-stage delay through the ALS04. You can make a specification table, such as time of about 30ns. Because through the GAL, there is a period of 45ns together, I think it is enough. Data is output from the DRAM is minute access time, since after the RAS since become active. The so-called fast that RAM, access time this means the short ones.
The timing table, I found that there is a margin of 15MHz pretty even those be of 10MHz. But, DRAM memory contents will be lost once it is read. Therefore, DRAM itself, but is to repair that was gone, I said precharge time the time it takes to repair it. Represents the minimum amount of time will reach the Low RAS RAS then after it becomes High, This is supposed to be about 60ns access time in DRAM of 80ns. One clock is 66.7ns at 15MHz. AS until High Low RAS has become, but because it is nearly one clock, I also seem quite dangerous if such thinking.
Become 60ns one clock is about 16.6MHz. Well, there will likely be a little margin, what does move up to about 17MHz in memory of 80ns. Different from the type of DRAM, its precharge time and access time is not said to be clear. (Which I think will be at high clock maybe) if the data is absolutely unstable, it will put a WAIT unfortunately. This works well as simply changing out the same as the CAS, the're designed to be the same as the output RAS DTACK. Now, WAIT I will enter only when it is not time for the output data. Never hurts to stable operation again.

## Refresh Timing

You also need towards the refresh timing. Since this is in addition to refresh the body side, enough to generate a timing issue in the RAS to CAS after the board side. Have created a delay in passing the three-stage 04 as well.
Hours, etc. CAS-RAS in this area varies from DRAM, I will make it for roughly. The thing is not to be too short in ALS04. At that time, please try with LS04.

## Check

Have finished the check on the board to complete the wiring, I finally connected.
Is set to 12M memory SWITCH.X etc. First, we re-launch.
What, do you have enough memory surprised by MEMFREE?
Then, run a memory check program, I examine whether there is memory corruption.
Let me bring up the OS-9 and SX-Window which are said to be tough and the next memory check. Board of those who stand up properly in this is okay. Congratulations.

## Troubleshooting

If you turn on the power, the body has become a strange behavior, they'll have to cut the power immediately. At that time, there is a possibility that the power supply does not fall in the above. When such would quickly pull off or the power outlet in the back.
I want to even if the strange smell and sparks came out. However, it might not rise again in that case ...
Although future measures to those who unfortunately was useless, in the case of the following symptoms it is raised.

| **Symptom** | **Countermeasure** |
|---|---|
| Sound of "Be" and to put the power on. | I have a short power. I said to be careful about that. |
| I would stop the display without being 31kHz when the power is turned on. I do not fall in the previous power. | DTACK relationship might be funny. I may or may not fall into the GND. |
| I come out "Please Reset". | There is a possibility that the data bus buffer funny. Signals such as G and is IDDIR be funny. Funny thing since you might reside SRAM, I also see the launch press OPT.1. |
| Check out the memory bus error. | DTACK is not returned. Check out the neighborhood. |
| I was caught in a memory check. | ($ 200000), I'll take a look at the contents of the memory using the debugger if the address of the first. If there is only FFFF, the control signal line is funny. RAM is not running or bus buffer.<br>If an error in the address in the middle comes out, is a matter of timing, such as noise. Or try increasing the capacitor, I will try to change the value of the damping |

| | |
|---|---|
| | resistor.<br>If you would change to a different address and write to a single address, the address lines are funny. Looking carefully address lines. You should know if you use the debugger, which addresses also wrong. |

## Then

For a little while, we'll tease around with memory as a pilot period had moved to say.
I think if you are still fully functional, and may be said to be complete.
However, I should not be relieved for half a year. May suddenly stop working one day.
In most cases, there seems to be a bad soldering.
So, what would I challenge the next ...

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